App. Serial No.: 09/051,263
Atty. Docket No.: 0081-012

REMARKS

These remarks are in response to the Office Action dated October 30, 2008, which has a shortened statutory period for response set to expire January 30, 2009. A three-month extension, to expire April 30, 2009, is requested in a petition filed herewith.

Claims

Claims 45-62 are pending in the above-identified application. Claims 1-12, 27-30, and 63-76 are withdrawn from consideration pursuant to a prior election/restriction requirement. Claims 45-62 are rejected over prior art. Claims 1-44 and 63-76 are canceled. Claims 45-62 remain as previously presented. Reconsideration is requested.

Rejections Under 35 U.S.C. § 102

Claims 45 and 54-62 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,292,668 (Miller et al.). The Examiner writes (in part):

> Referring to claim 45, Miller has taught a microprocessor system, comprising:
>
> ...
>
> g. an external CMOS oscillator, operating in conjunction with a clock multiplier (Miller column 24, line 35 to column 26, line 35); ...

Applicants respectfully traverse.

The standard for anticipation is set forth in M.P.E.P. § 2131 as follows:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Miller et al. does not disclose "an external CMOS oscillator, operating in conjunction with a clock multiplier" as recited (in part) by Claim 45. Rather, Miller et al. shows an internal clock 281 in FIG. 8 that is part of the central processing unit 200 shown in FIG. 3 (*Miller et al.*, col. 18, lines 16-26; FIGs. 3 and 8). As indicated at column 22, lines 62-64 of Miller et al., "[c]lock 281 provides the various timing signals (PTIME0 through PTIME4 and BCYCOT) used

throughout the system (see FIGS. 14 and 15)." The components of clock 281 are further shown in FIGs. 14 and 15 and are further described at col. 24, line 36 to col. 26, line 35 in Miller et al. Additionally, there is no indication that the clock 281 operates "in conjunction with a clock multiplier" as recited by Claim 45.

Because Miller et al. does not disclose all the limitations of Claim 45, Miller et al. does not anticipate Claim 45. Claims 54-62 depend, either directly or indirectly, from Claim 45 and are, therefore, distinguished from the cited prior art for at least the same reasons provided above with respect to Claim 45.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of the rejections under 35 U.S.C. § 102.

Rejections Under 35 U.S.C. § 103

Claims 46-47:

Claims 46-47 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 4,292,668 (Miller) in view of U.S. Patent No. 4,321,706 (Craft).

Applicants respectfully traverse.

Each of Claims 46-47 depends directly from Claim 45 and, therefore, includes all the limitations of Claim 45. As indicated above, Miller et al. does not teach or suggest "an external CMOS oscillator, operating in conjunction with a clock multiplier" as recited by Claim 45. Similarly, Craft does not appear to teach or suggest such an element. Therefore, because the cited prior art do not teach or suggest all the limitations of either of Claims 46-47, no prima facie case of obviousness is established with respect to Claims 46-47.

Claims 48-50:

Claims 48-50 are rejected under 35 U.S.C. § 103 as being unpatentable over Miller in view of Official Notice.

Applicants respectfully traverse.

Each of Claims 48-50 depends directly from Claim 45 and, therefore, includes all the limitations of Claim 45. As indicated above, Miller et al. does not teach or suggest "an external CMOS oscillator, operating in conjunction with a clock multiplier" as recited by Claim 45.

Therefore, because the cited prior art does not teach or suggest all the limitations of any of Claims 48-50, no prima facie case of obviousness is established with respect to Claims 48-50.

In addition, Applicants respectfully object to the Examiner's taking official notice of Claims 48-50. MPEP § 2144.03(A) provides (in part) the following:

> Official notice without documentary evidence to support an examiner's conclusion is permissible only in some circumstances. While "official notice" may be relied on, these circumstances should be rare when an application is under final rejection or action under 37 CFR 1.113. Official notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known. As noted by the court in *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970), the notice of facts beyond the record which may be taken by the examiner must be "capable of such instant and unquestionable demonstration as to defy dispute."

Claim 48 recites (in part) that "said MPU retrieves up to four instructions from memory for each instruction fetch or pre-fetch." The Examiner takes official notice of Claim 48 because "[a] person of ordinary skill in the art at the time the invention was made would have recognized that increasing the number of instructions fetched improves processor efficiency, since it decreases the amount of time needed to fetch the instructions." Despite this assertion, the Examiner provides no indication of how the device of Miller et al. could or would be modified to include the limitations of Claim 48, even though the Examiner notes that Miller et al. does not teach or suggest the limitations of Claim 48.

Claim 49 recites (in part) that "said MPU fetches multiple sequential instructions from said global memory unit in parallel, and said global memory unit supplies said multiple sequential instructions to said MPU during a single memory cycle." The Examiner takes official notice of Claim 49 because "[a] person of ordinary skill in the art at the time the invention was made would have recognized that increasing the number of instructions fetched in a single cycle improves processor efficiency, since it decreases the amount of time needed to fetch the instructions." Despite this assertion, the Examiner provides no indication of how the device of Miller could or would be modified to include the limitations of Claim 49, even though the Examiner notes that Miller et al. does not teach or suggest the limitations of Claim 49. Furthermore, Claim 49 states that the MPU fetches instructions "in parallel" and that "said global

memory unit supplies said multiple sequential instructions to said MPU during a single memory cycle." The Examiner does not address these additional limitations in the rejection of Claim 49.

Claim 50 recites (in part) that "said MPU further comprises an arithmetic logic unit (ALU) that is used for data operations and for branch address calculations." The Examiner takes official notice of Claim 50 because "[a] person of ordinary skill in the art at the time the invention was made would have recognized that executing data operations and branch address calculations increases compatibility, Since more instructions can be executed." Despite this assertion, the Examiner provides no indication of how the device of Miller could or would be modified to include the limitations of Claim 50, even though the Examiner notes that Miller et al. does not teach or suggest the limitations of Claim 50.

Finally, Applicants note that the present application claims priority to a provisional application filed in 1995. Given the age of this priority application, Applicants respectfully aver that the limitations of Claims 48-50 would not have been so obvious to a person of ordinary skill at the time the invention was made "as to defy dispute."

For the above reasons, Applicants respectfully aver that it is improper for the Examiner to take judicial notice of Claims 48-50. Therefore, should the Examiner wish to maintain the rejections of Claims 48-50, Applicants respectfully request that the Examiner provide additional evidence on the record supporting an obviousness rejection of Claims 48-50.

Claims 51-52:

Claims 51-52 are rejected under 35 U.S.C. § 103 as being unpatentable over Miller in view of U.S. Patent No. 5,070,451 (Moore et al.). Claim 53 is rejected under 35 U.S.C. § 103 as being unpatentable over Miller and Moore in view of Official Notice.

Claims 51-53 depend, either directly or indirectly, from Claim 45 and, therefore, include all the limitations of Claim 45. As indicated above, Miller et al. does not teach or suggest "an external CMOS oscillator, operating in conjunction with a clock multiplier," (emphasis added) as recited by Claim 45. Similarly, Moore et al. does not teach or suggest these limitations. Therefore, because the cited prior art does not teach or suggest all the limitations of any of Claims 51-53, no prima facie case of obviousness is established with respect to any of Claims 51-53.

Furthermore, Applicants respectfully object to the Examiner taking official notice of the limitations of Claim 53 because the Examiner has not indicated how such the limitations of Claim 53 could be incorporated into the combination of Miller et al. and Moore et al. Furthermore, due to the age of the priority application, Applicants respectfully aver that the noticed limitations of Claim 53 were not "capable of instant and unquestionable demonstration" at the time the invention was made "as to defy dispute." Therefore, Applicants respectfully aver that it was improper for the Examiner to take judicial notice of Claim 53. Should the Examiner wish to maintain the rejections of Claim 53, Applicants respectfully request that the Examiner provide evidence on the record supporting an obviousness rejection of Claims 53.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of all the rejections under 35 U.S.C. § 103.

For the foregoing reasons, Applicants believe that Claims 45-62 are in condition for allowance. Should the Examiner undertake any action other than allowance of Claims 45-62, or if the Examiner has any questions or suggestions for expediting the prosecution of this application, the Examiner is requested to contact Applicants' attorney at (269) 279-8820.

Respectfully submitted,

Date: 4/30/09

Larry E. Henneman, Jr., Reg. No. 41,063
Attorney for Applicant(s)
Henneman & Associates, PLC
714 W. Michigan Ave.
Three Rivers, MI 49093

CERTIFICATE OF FACSIMILE TRANSMISSION (37 CFR 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being transmitted via facsimile, on the date shown below, to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, at (571) 273-8300.

Date: 4/30/09

Larry E. Henneman, Jr.